

Computer Architecture Fall 2003

Open Book and Notes

Please answer both questions on this examination. The text referred to here is "Computer Architecture: A Quantitative Approach", Third Edition, by J.L. Hennessy and D. A. Patterson. Please make sure that your answers are written clearly. State any assumptions you make in your answers.

1. We compare the computation and memory access times of two processors. The first is a 2 GHz processor with a 64 KB, 2-way associative data cache, and a cache block size of 64 bytes. The second is a 731 MHz processor with an 8 KB direct mapped data cache with 32 byte cache blocks. The cache miss rate (per instruction) for the first processor is 0.031, while the cache miss rate for the second is 0.068; the cache miss penalty is 88 cycles for the 64 KB cache with 64 byte blocks, while it is 84 cycles for the 8 KB cache with 32 byte blocks. Assume that the cache hit time is 1 cycle, and the average CPI is 2, for both machines.

What is the ratio of performance of the two machines, if one computes performance solely from the clock rates of the processors? The performance of many scientific computing programs is determined primarily by their memory access times. Calculate the expected ratio of performance for the two processors, if memory access times dominate.

2. A segment of MIPS code is given below. This code embodies a loop over vectors of length "N" (a numerical value) and computes

$$S = S + A \times X[j] + Y[j]$$

for $j = 1, 2, \dots, N$.

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                                ADD.D    F0,R0,#0    ; S = 0
                                DADDUI   R4,R0,#1    ; Counter R4 = 1
foo:  L.D      F2,0(R1)         ; load X[j]
                                L.D      F4,0(R2)         ; load Y[j]
                                MULT.D   F2,F6,F2      ; A × X[j]
                                ADD.D    F2,F2,F4      ; A × X[j] + Y[j]
                                ADD.D    F0,F0,F2      ; S = S + A × X[j] + Y[j]
                                DADDUI   R1,R1,#8      ; increment X index
                                DADDUI   R2,R2,#8      ; increment Y index
                                DADDUI   R4,R4,#1      ; Increment counter R4
                                DSGTUI   R3,R4,N       ; R4 > N?
                                BEQZ     R3,foo        ; Branch if R3 = 0

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The DSGTUI instruction sets $R3 = 1$ if $R4 > N$, else $R3 = 0$. The meaning of the other instructions is obvious. The architecture of a processor is that shown in Figure 3.2 of the text with the addition of an integer EX unit. The control uses Tomasulo's algorithm. The number of cycles required for execution is 1 for the integer EX unit which executes all integer arithmetic and logic instructions, 1 for the address unit which computes addresses for all loads and stores, 1 for the memory unit, 4 for the floating point add unit, 7 for the floating point multiply units and 15 for floating point divides

which execute in the floating point multiply unit. Only one result can be written to the CDB in each cycle.

- (a) Assume that this is a single issue Tomasulo control with branch predict taken, but no speculation. Show the execution of the first 2 iterations of the loop in the format of Figure 3.25 of the text.
- (b) Assume that this is a two-issue Tomasulo control with branch predict taken and speculation. Show the execution of the first 2 iterations of the loop in the format of Figure 3.25 of the text.