Question Code P/ARCH

Diagnostic Exam Fall 2003

Architecture Paper

This examination is based on Chapter 5 of *Parallel Computer Architecture*, by Culler and Singh. Please answer both questions.

1. (a) Explain briefly the difference between cache coherence and serial consistency.

   (b) Consider the following proposed sufficient conditions for serial consistency.

   - Every processor issues memory requests in program order.
   - After a memory operation is issued, the issuing processor waits for that operation to complete before it issues another memory operation.
   - A processor P_j returns a value written by another processor P_i only after all memory operations that were performed with respect to P_i before it issued the write have performed also with respect to P_j.

   Do these three conditions guarantee serial consistency? If so, state your reasons. If not, give a counter-example, and show that the the conditions in the text book guarantee serial consistency.

2. Suppose P processors of a bus-based shared memory multiprocessor try to acquire a lock once each, simultaneously. Assume that initially the first processor has the lock, and that the other processors are spinning on the lock. Assuming that the bus is fair, what is the worst-case number of bus transactions needed until all processors have acquired the lock once each, for the three cases:
   (1) a test-and-test-and-set lock,
   (2) an array lock,
   (3) a ticket lock?