CALL FOR PAPERS

Workshop on Advances in Parallel Computing Models

to be held in conjunction with

International Symposium on Parallel Architectures, Algorithms and Networks
June 23-25, 1999
Perth, Australia

The past twenty years have seen a flurry of activity in the arena of parallel algorithms. Most of these algorithms were developed in the PRAM model, which assumes synchronous processors having access to shared memory. The PRAM model has turned out to be an excellent theoretical model that focuses on algorithm development at the expense of implementation details. Not surprisingly, a wealth of fundamental algorithms and algorithmic paradigms have been developed for the PRAM. However, the PRAM is not a practical model.

On the other hand, new parallel and computing models have been proposed to reflect advances in new computational devices and environments such as optical interconnects, FPGA devices, networks of workstations, radio communication, etc. New algorithmic techniques and paradigms have been recently developed for the new models.

The main goal of this workshop is to provide an important forum for the dissemination and exchange of new ideas, techniques and research in the field of the new models of parallel computing reflecting new devices and practical situation. The workshop will bring together researchers and practitioners interested in all aspects of parallel computing theory. The workshop atmosphere will be conducive of open and mutually beneficial exchanges of ideas between the participants.

Topics of interest include, but are not limited to:

o Models of parallel computing

- Bulk Synchronous Parallel (BSP) model
- LogP model
- Coarse grained multicomputer (CGM) model
- Reconfigurable model
- Optical model
- Asynchronous model
- Broadcast communication model
- Network models
- Hardware-specific models

o Fundamentals and algorithms:

- Geometric and graph algorithms
- Combinatorial algorithms
- Randomized and approximation techniques
- Numerical algorithms
- Distributed algorithms
- Image Processing

o Practical aspects and applications:

- Implementation and performance analysis
- PVM/MPI
- Development tools
- Visualization
- Compiler
- Fault tolerance

The workshop proceedings will be published by IEEE Computer Society Press. The proceedings will be available at the workshop.

Submission Guidelines:

Please submit an electronic version of an original, unpublished manuscript, not to exceed 10 single-spaced pages, to one of the Program Co-chairs by email (see below). All manuscripts will be reviewed. Submissions should be in Postscript (level 2) format. Authors should make sure that the submission can be viewed using ghostscript and will print on a Postscript printer that uses standard letter size paper (8.5" x 11"). Submissions must be received by February 1, 1999.

Important Dates:

- Manuscript due February 1, 1999.
- Notification of acceptance/rejection by March 1, 1999.
- Final version due March 15, 1999.

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